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Ion implanted silicon-electrolyte interface

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A silicon surface implanted with energetic ions was studied by measurements of the impedance and current–voltage characteristics using the semiconductor–electrolyte (SC–EL) interface. The results are in accordance with the known data from experiments on solid state structures. A great sensitivity to surface damage due to ion implantation was found for the SC–EL system, which thus provides a new tool for characterizing surface properties of Si after ion implantation.

1. Introduction

In ion implanted device applications, the damage introduced by bombardment with energetic ions is of considerable importance. Frequently, the damage may affect decisively the properties of ion-implanted devices. Thus, information about the damage formation and the depth distribution of such damage is essential to the device fabrication. The problem of implantation damage was explored in the past using electrical and crystallographic methods on all-solid state structures [1–3].

It is well known that the interface SC–EL bears a great similarity to a semiconductor–metal interface (SC–M) and has been usefully applied to study the properties of both the EL and the SC [4, 5]. If precautions are made to minimize the process on the EL side, information on the SC side can be obtained. Due to the fact that the Helmholtz capacitance (equivalent to oxide capacitance in MIS structure) is very large, a high electric field can be applied to the SC.

With the purpose of clarifying whether the interface SC–EL is sensitive to ion implantation damage we have carried out impedance measurements and current–voltage measurements. Emphasis is placed on the correlation of the observed behaviour with the known data obtained by other techniques in order to adopt the SC–EL interface for characterizing surface damage created by ion implantation.

2. Experimental

2.1 *Samples*

The specimens used were $< 111 >$ silicon slices (18 mm in diameter and 0·3 to 0·5 mm thick). The material was *p*- and *n*-type and 10 to 100 Ω cm. Prior to implantation the samples were mechanically lapped and polished down to 0·25 μm with diamond paste. The polishing (on one side) was followed by a 3 min etch in a $HF:HNO_3:CH_3COOH$ mixture to remove (about 60 μm) the mechanical damage. The polished face was implanted for studying the effect of the implantation. The implantation energy was 30 keV and the dose in the range 10^{11} to 10^{15} ions cm^{-2}. Implantations were conducted with the samples misoriented by 8° to avoid channelling. A Teflon mask provides a defined surface area for exposing to the electrolyte (0·15 cm^2).

The back face of the sample was exposed to a high dose implantation (n^+ on *n*-Si and p^+ on *p*-Si) and evaporated with Al to achieve the ohmic contact.

2.2. *Circuit*

Fig. 1 shows schematically the electrical circuit. The electrochemical cell is built with Si as the working electrode (we) and Pt as the counter electrode (ce), 2.2 N HF in 0.5 M Na_2SO_4 being the electrolyte. A saturated calomel electrode (SCE) was employed as a reference electrode to monitor

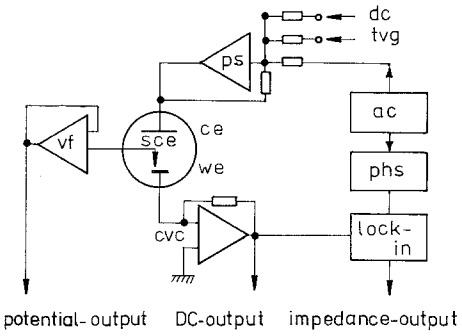

Fig. 1. Block diagram: ce = counter electrode, we = working electrode, sce = saturated calomel electrode, vf = voltage follower, cvc = current–voltage converter, ps = potentiostat, dc = voltage supply, ac = oscillator, phs = phase shifter, lock-in = lock-in amplifier.

the potential of the we. The potential between we and ce was held close to that set up on a reference voltage source (triangular). The d.c. current passing through the sample was measured in the usual way by means of a current voltage converter (cvc). For measuring the impedance a small a.c. voltage (5 mV peak to peak) was superimposed via a potentiostat (ps) on the triangular voltage. The corresponding alternating current, after passing the cvc, was supplied to the lock-in amplifier (1.5 Hz to 150 kHz), which operated in these measurements as a vector meter (two lock-in amplifiers were needed to obtain the components of the impedance; this is not shown in Fig. 1). Thus, the resistive component and the capacitive component of the electrode impedance could be plotted on a $X-Y$ recorder as a function of the electrode potential.

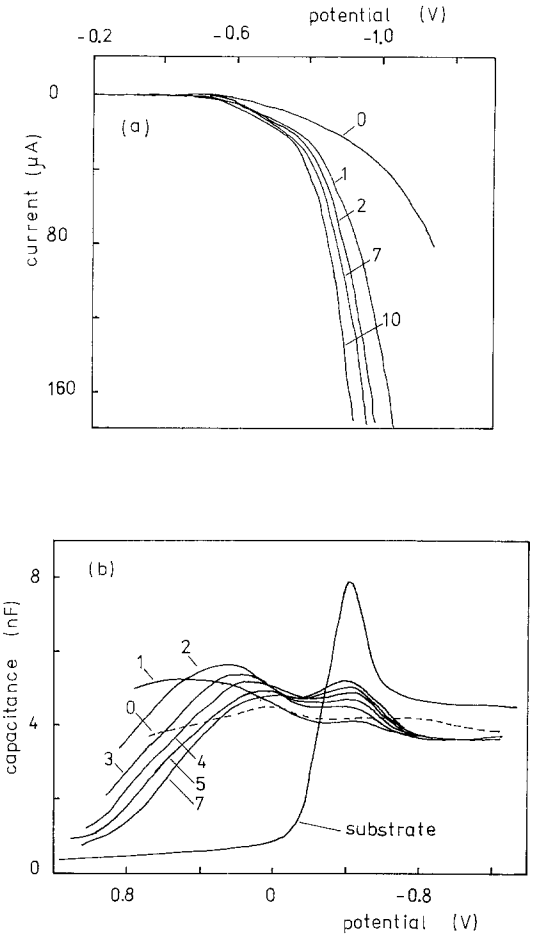

Fig. 2. Characteristics of an n-Si surface (100 Ω cm) implanted with 10^{13} P cm^{-2} at 30 keV: (a) forward current versus voltage; (b) capacitance versus reverse bias. The number indicates the removed layer (× 100 Å).

2.3 *Procedure*

The potential of the we was swept at a constant rate (0·2 V s^{-1}) between pre-set potential limits: rest potential–cathodic going–rest potential–anodic going–rest potential.

The corresponding response, impedance and d.c. current were recorded. This operation was repeated after each layer etching. Measurements were carried out at 25 + 0·2° C and in the dark. The results described below were taken at a frequency of 60 kHz.

3. Results

The general behaviour of the ion implanted surface is shown in Figs. 2–6. For comparison the characteristics of non-implanted surfaces are also included in all these Figures. The impedance component C_p (parallel circuit) is shown in Fig. 2, as a function of the electrode potential U_e for an n-Si electrode implanted with 10^{13} P cm^{-2}. The step in the $C_p - U_e$ traces is seen to broaden with respect to the non-implanted specimen. A maximum is observed in the reverse bias range. The successive layer etching causes the traces to move towards the curve characteristic of the non-implanted surface. The layer etching was made galvanostically in the same measured electrolyte; the sample being biased anodically for a desirable duration. Precautions were taken to prevent the surface film formation during the etching (small current

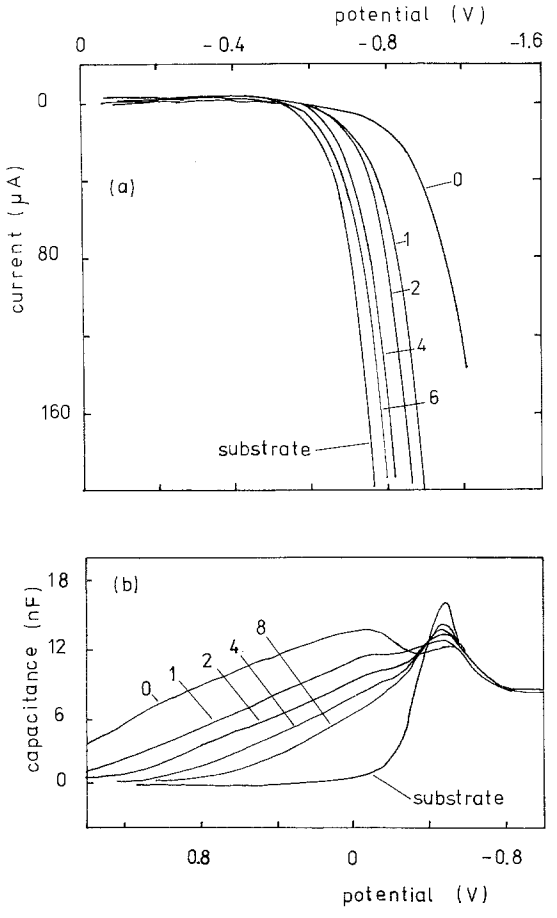

Fig. 3. Characteristics of an *n*-Si surface (100 Ω cm) implanted with 2×10^{12} A s cm^{-2} at 50 keV: (a) forward current versus voltage; (b) capacitance versus reverse bias. The number indicates the removed layer (× 100 Å).

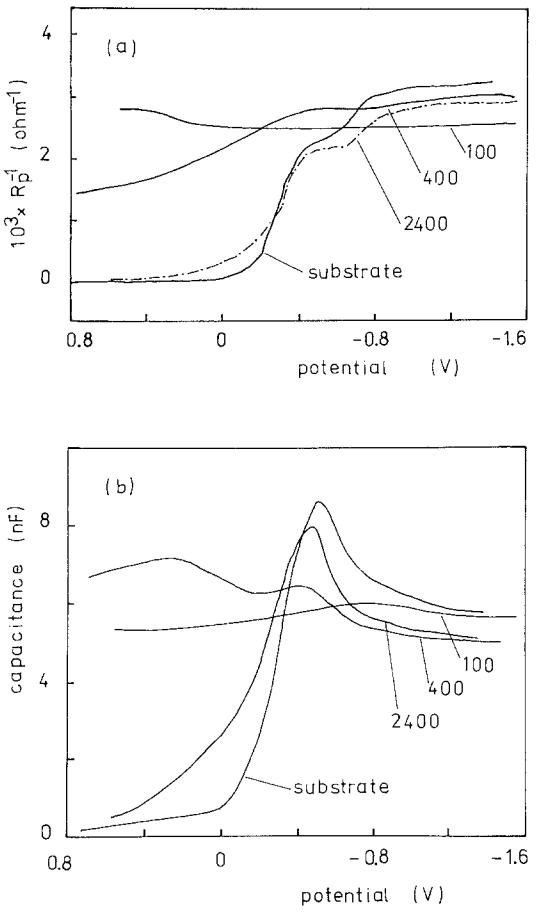

Fig. 4. Characteristics of an *n*-Si surface (100 Ω cm) implanted with 10^{15} P cm^{-2} at 30 keV: (a) $1/R_p$ versus potential; (b) capacitance versus potential. The number indicates the removed layer (Å).

density, stirring, illumination), although the surface films observed in some cases did not appear to influence the measurement.

The thickness of the removed layer was calculated from the electricity used and the wafer geometry assuming a 100% current yield and the divalent state of Si for the anodic dissolution [6]. The results obtained by electrochemical etching differed insignificantly from those after chemical etching. The chemical stripping was conducted in a solution of 0·075 wt.% HF in HNO_3 which enabled an etch rate of 50 Å min^{-1} at 30° C [7]. The effect caused by ion implantation appears also in the current–voltage characteristics. A readily increased current in the reverse bias direction is typical. In the forward bias direction, however a reduction in the current is observed, Figs. 2, 3 and 6. The successive layer etching revealed again the behaviour of the non-implanted surface. The resistive component $1/R_p$ of the impedance is presented in Figs. 4 and 5. It follows essentially the current–voltage behaviour: large values for $1/R_p$ are seen in the potential region where the d.c. current readily passes across the interface and vice versa.

The degree of deviation from the non-implanted surface increases with increasing doses, as seen from Figs. 2 and 4. The nature of the ion species seems to cause insignificant effects, since similar behaviour with samples exposed to implantation with different ions, e.g. As, P, C, Si, B was found.

4. Discussion

There are several possible reasons for the deviation

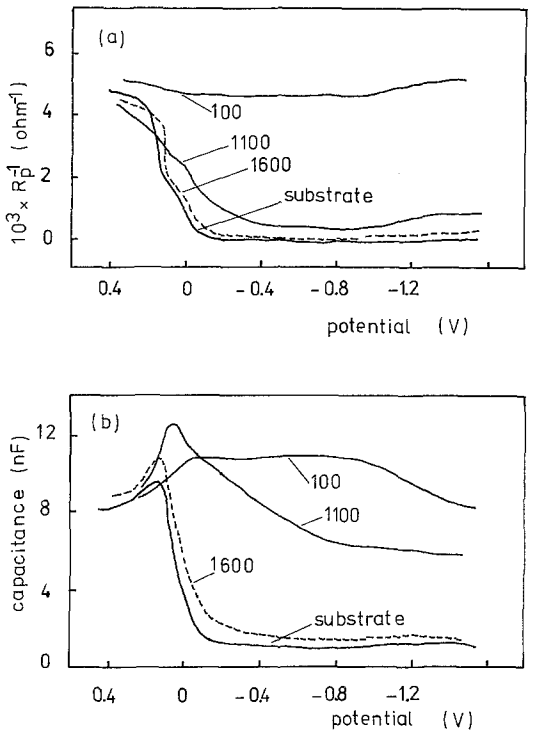

Fig. 5. Characteristics of a p-Si surface (10 Ω cm) implanted with 10^{15} B cm^{-2} at 30 keV: (a) $1/R_p$ versus potential; (b) capacitance versus potential. The number indicates the removed layer (Å).

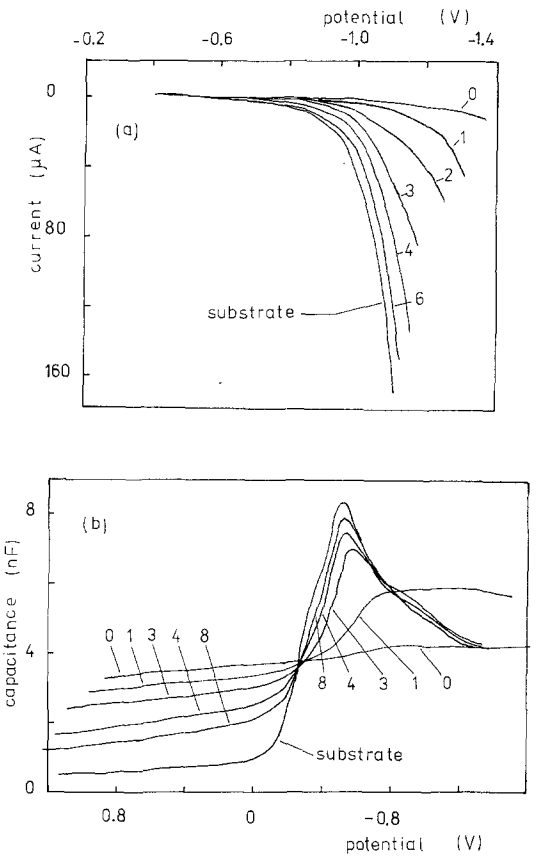

Fig. 6. Characteristics of an electron deposited amorphous Si surface: (a) forward current versus voltage, (b) capacitance versus voltage. The number indicates the removed layer (× 100 Å).

in the behaviour of the implanted surface from that of non-implanted surfaces. The implantation dopes the substrate and thus changes the carrier density in the surface layer. Meek [8] found that n^+-Si is readily dissolved anodically in HF solutions and explained this effect by the surface generation enhanced by tunnelling. In our experiments the doping was intentionally suppressed, since the samples were not annealed after implantation. The doping is perhaps not excluded in the large dose range, where the temperature during the implantation was not maintained at room temperature. Due to the fact that the implantation of Si ions into a Si substrate, where the doping is excluded, showed specific behaviour as also did other implantation ions, we conclude that the observed effects can be attributed to the induced damages.

4.1. *Generation – recombination of carriers*

The bombardment by energetic ions produces serious damage in the crystal lattice, if the sample is not annealed afterwards. Even after annealing treatment, a significant amount of damage remains and in high dose implantation quantitative removal of damage cannot be achieved. This behaviour has been studied and discussed widely in the literature for solid state structures [1–3].

The single crystal silicon–electrolyte interface (Si–EL) behaves similarly to a SC–M system or to an asymmetrical p–n junction [4, 5]. In the reverse bias direction the Si–EL interface is characterized by the blocking current and by the depletion capacitance due to the passing of minority carriers across the interface (e.g. holes for n-Si). These well-known characteristics for the Si–EL interface are changed profoundly after the surface is exposed to the ion implantation, even at doses as low as 10^{11} ions cm^{-2}, as presented in the foregoing section.

The increase in the depletion capacitance sug-

gests the presence of localized levels in the forbidden energy gap. This can be due to surface states or bulk states. The behaviour of the capacitance (shape, magnitude, continuous change with potential) with respect to the layer etching, forces us to conclude that the surface states are indistinguishable from the bulk states. Thus, the bulk states of N_t ($cm^{-3}\,eV^{-1}$) contribute to $N^{2/3}$ ($cm^{-2}\,eV^{-1}$) at the surface and the measured capacitance is mainly due to that of space charge, reflecting the contribution of deep levels due to damage introduced by ion implantation. The maximum capacitance in the reverse region appears at an electrode potential of about 0·2 V, independent of the dose and the ion species. This potential is identical with the potential where the maximum in capacitance is observed in a non-implanted *p*-Si electrode and already verified by Memming and Schwandt [9] as the recombination–generation level. For *n*-Si this level is usually not visible in the capacitance behaviour due to the strong interaction of the latter with the valence band and the anodic dissolution current removes all holes necessary for the redistribution of carriers in the surface states.

In the case of implanted *n*-Si it is believed that a large amount of introduced damage produces recombination–generation centres increasing drastically the minority carrier density so that the limiting process shifts towards the electrolyte side. In addition, the capture coefficients for electrons and holes by damage may also change after implantation. The observed reverse current in the region of the capacitance maximum is not limited, indicating that enough holes are available. At small doses the maximum does not appear at 0·2 V, Fig. 3. Generation provides holes which are utilized by the anodic process. This is evident from the reverse current at low implantation doses, which shows signs of saturation. The presence of a large density of generation–recombination centres is obvious also from the lack of the photovoltaic effect for implanted samples. The strong interaction of the damage centres with the minority carriers generated by illumination decreases greatly the lifetime of the latter so that no carrier separation in the interface field Si–EL occurs, which is observed normally in the shift of the rest potential upon illumination on non-implanted surfaces. Details of this subject will be published.

We conclude that the observed capacitance maximum in the reverse bias region is related to the mid-gap states. They are similar to those visible on non-implanted *p*-Si and are responsible for the increase in the reverse current. It is believed that these mid-gap states, which are independent of the ion species, have the same origin as that of the generation–recombination levels observed by Ashburn and Morgan [10] on *p–n* junctions bombarded with C ions.

4.2 *p-i-n junction formation*

The cathodic current of the system Si–EL is due to the reaction of hydrogen ions with the conduction band electrons in the semiconductor, unless other oxidizing agents are present in the electrolyte. In acid solution the stationary current depends then on the electron concentration at the SC surface. The result of this is that *n*-Si is able to pass cathodic current readily and *p*-Si is not. The observed decrease in cathodic current (forward bias on *n*-Si) on implanted electrodes strongly suggests the removal of electrons by surface damage, the degree of which depends on the implantation dose. Indeed, the decrease in electron concentration on Si samples subjected to ion implantation has been found [11–16]. Gossick [14] explained this effect in terms of the acceptor character of the introduced damage resulting in a charge compensation. The consequence of this is the formation of an *i*-type layer on the substrate. More recently, Ashburn and Morgan [10] have successfully clarified the behaviour of *p–n* junctions, damaged with a carbon ion beam, using the concept of charge compensation.

Following Ashburn we assume that a damaged layer is formed on the substrate, the resistivity of which increases with implantation dose and at higher doses this layer is converted into *i*-type. Thus the interface of our system can be described by a structure p^+-*i*-*n* (for *n*-Si substrate) where p^+ represents the electrolyte side, as depicted in Fig. 7. If the interface is biased cathodically, electrons are injected from the *n*-region into the *i*-region. Due to the presence of a high defect concentration in the *i*-region the mobility of current carriers is low and the recombination rate is high resulting in a lowering of the carrier flux across the interface. The above explanation conforms to the observed

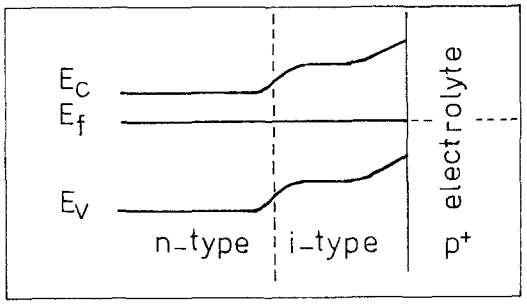

Fig. 7. Energy diagram of a heavily damaged Si surface in contact with an electrolyte.

reduction of the cathodic current. On the other hand, the reverse current increases drastically at high implantation doses, correlating well with the p^+-*i*-*n* model. It is known that the anodic dissolution of *n*-Si increases with increasing resistivity [17].

The behaviour of the capacitance of the interface in the forward bias region is mainly determined by the process of hydrogen reduction. The decrease in the capacitance at high cathodic voltage is not due to the conductivity modulation but is caused by hydrogen covering, as found by Gobrecht and Meinhardt [18] in the system Ge–electrolyte. However, at reverse bias the capacitance changes slowly, especially at high implantation doses indicating the behaviour of a *p*-*i*-*n* structure and that in addition to mid-gap states other deep levels are present too. A series of deep levels introduced by ion implantation into the Si surface have been observed by Urli [12], Davies and Roosild [11] and by Ashburn and Morgan [10] from thermo-stimulated current measurements. The low capacitance voltage traces in our experiments show no signs of single energy levels. This may be due to a high density of the mid-gap states so that other levels are masked. However, it seems reasonable to assume a continuous distribution of traps, especially at implantation doses which are high enough to make the surface layer amorphous, since such a distribution has been observed on amorphous Si [19], produced by electron beam deposition.

For comparison the capacitance and forward current as a function of bias for an amorphous Si-surface are shown in Fig. 6. The amorphous surface was produced by electron beam deposition of pure Si on to a Si substrate (1500 Å). The similarity between these results and those obtained by ion implantation is seen. The increase in the capacitance at reverse bias, similar to that observed previously, is due to the deep levels which are continuously and uniformly distributed throughout much of the forbidden gap.

5. Conclusion

We have shown that measurements on SC–EL interfaces can yield similar information about the lattice damage present after ion implantation as obtained by other techniques. The electrochemical method provides a new tool for characterizing implantation damage in Si. On the basis of these results methods can be developed [20, 21] to characterize the properties of ion-implanted Si surfaces. The system SC–EL has the advantage that the measurement techniques and required apparatus are not complicated. The sensitivity is high, since surface effects caused by ion bombardment with doses as low as 10^{11} ions cm^{-1}, are large enough to be detected.

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